

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claim 27 without prejudice.

- 1 1. (Previously Presented) A method comprising:
 - 2 testing a duty cycle of a random bit source;
 - 3 varying an output voltage of a voltage source if the duty cycle has not
 - 4 substantially reached a first threshold; and
 - 5 iteratively altering the output voltage of the voltage source until the duty cycle has
 - 6 not substantially reached the first threshold.

- 1 2. (Original) The method of claim 1 further comprising:
 - 2 periodically latching a high frequency signal in response to a low frequency
 - 3 signal; and
 - 4 outputting one or more binary digits corresponding to a voltage level of the
 - 5 latching high frequency signal.

- 1 3. (Previously Presented) The method of claim 1 wherein varying the output
2 voltage of the voltage circuit further comprises updating a threshold voltage of a flash
3 memory cell in the voltage circuit.

- 1 4. (Original) The method of claim 1 wherein varying the output voltage of the
2 voltage circuit further comprises:
 - 3 varying an input current to a non-inverting input of a differential amplifier to
 - 4 produce a first input voltage; and
 - 5 varying an input current to an inverting input of the differential amplifier to
 - 6 produce a second input voltage.

1 5. (Original) The method of claim 1 wherein varying the output voltage of the
2 voltage circuit further comprises altering the number of transistors in the voltage circuit
3 determining the output voltage.

1 6. (Original) The method of claim 1 wherein the method of producing a uniform
2 duty cycle output from a random bit source is used in a random number generator
3 operable to produce random binary numbers for use in a cryptographic system for secure
4 communications between a plurality of computers in a network.

7-24. (Cancelled)

1 25. (Previously Presented) The method of claim 1 wherein the first threshold is
2 fifty percent.

1 26. (Previously Presented) A random bit source comprising:
2 a latch to produce a uniform duty cycle output;
3 a component to test the duty cycle; and
4 a programmable voltage source to vary an output voltage if the duty cycle has not
5 substantially reached a first threshold and iteratively alter the output voltage until the
6 duty cycle has not substantially reached the first threshold.

27. (Cancelled)

1 28. (Previously Presented) The random bit source of claim 26 wherein the
2 programmable voltage source comprises a flash memory cell, wherein varying the output
3 voltage of the voltage circuit further comprises updating a threshold voltage of the flash
4 memory cell.

- 1 29. (Previously Presented) The random bit source of claim 26 wherein the
2 programmable voltage source further comprises differential amplifier, wherein varying
3 the output voltage of the programmable voltage source further comprises varying an input
4 current to a non-inverting input of the differential amplifier to produce a first input
5 voltage and varying an input current to an inverting input of the differential amplifier to
6 produce a second input voltage.
- 1 30. (Previously Presented) The random bit source of claim 26 wherein varying
2 the output voltage of the programmable voltage source further comprises altering the
3 number of transistors in the programmable voltage source determining the output voltage.
- 1 31. (Previously Presented) The random bit source of claim 26 wherein
2 producing a uniform duty cycle output from the random bit source is used in a random
3 number generator operable to produce random binary numbers for use in a cryptographic
4 system for secure communications between a plurality of computers in a network.
- 1 32. (Previously Presented) The random bit source of claim 26 wherein the first
2 threshold is fifty percent